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Gate all around MOSFET

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Abstract
To keep performance levels high, we've scaled down single-gate MOSFETs to nanometres over the last three decades or so, but they're still plagued by issues such as interface coupling and channel orientation as well as leakage current and latch-up. In addition, additional parameters such as short channel effects (DIBL, GIDL), body effect, hot electron effect, punch through effect, surface scattering, impact ionisation, sub threshold swing, and volume inversion have shown results in terms of an increase in leakage current, a decrease in inversion charge, and a decrease in the drive current since the double-gate MOSFET came into existence. Comparing double- and single-gate MOSFET design, this article evaluated several performance parameters and channel material configurations for both configurations and also analysed different channel materials along with its structural orientation and the future uses of these devices.

Keywords: Scaling, double-gate, MOSFET, short channel effects, volume inversion

Introduction
There was a need in the early 1930s for a device that could potentially replace large-sized Vacuum Tubes that were expensive, slow to operate, and consumed a lot of power. The concept of FETs (Field Effect Transistor) was born out of this need. However, FETs do not effectively demonstrate structure because surface states were present at the interface of semiconductor and oxide, preventing an electric field from entering the semiconductor matrix [1].

Combining three layers of metals (M), oxide (O), and semiconductor (S) on top of a grown silicon dioxide (SiO2) layer on the surface of the semiconductor allows electric field to enter into semiconductor material and gives rise to new invention concept named Silicon (Si) based MOSFETs (Metal Oxide Semiconductor Field Effect Transistors) with a single-gate configuration (SG-MOSFET) as shown in Fig.1. 1. Because of their high value and rarity as early 1960s building blocks, MOSFETs are still used as fundamental switching components in the area of ICs today while maintaining a basic structure that is very close to an early 1960s design [2, 3]. When Moore's Law was initially presented, it said that the number of transistors in a device would double every 18 months.
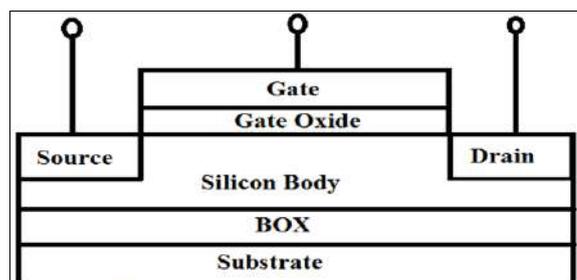

Fig 1: Single-Gate Configuration of MOSFET

An increasing number of transistors may be accommodated by increasing the size of a specific region, as illustrated in Figure 2.
In order to replace the current single-gate MOSFET, researchers have been focusing on finding the most efficient chips with higher speeds, low power consumption, and higher carrier mobility, as well as lowering transistor costs per chip by using non-Si materials that have capabilities like higher carrier mobility, high speed device applications, and low power consumption [3-8].

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The need to reduce power usage and dissipation. There are several dimensions characteristics that have an impact on the device, but all of them are reduced in Table I when considering device scaling. Scaling's primary benefits include.

1. Increased packing density
2. Enhancement of chip performance.
3. Cost-Effectiveness is improved.
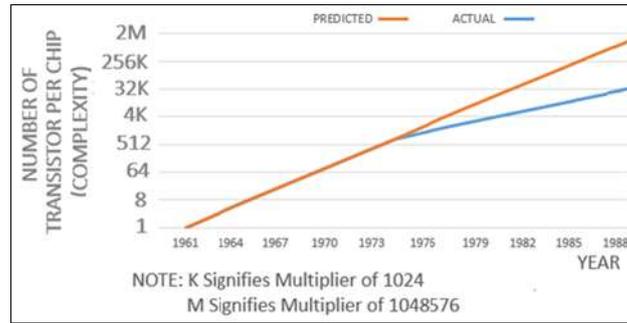4. Delays at the gate are reduced.
5. Frequency's working range expands

Fig 2: Moore's Law

Table 1: Scaling Parameters

Device Specifications	Notation	Scaling done at Constant Electric Field	Scaling done at Constant Voltage
Length of Channel	L	μ-1	μ-1
Width of Channel	W	μ-1	μ-1
Capacitance of Gate	CG	μ-1	μ-1
Capacitance of Oxide	COX	μ	μ
Electric Field	E	Constant	μ
Transit Frequency	FT	μ	μ2
Current	I	μ-1	μ
Substrate Doping	NA	μ2	μ2
Power	P	μ-2	μ
Oxide Thickness	TOX	μ	μ-1
Transit Time	TT	μ-2	μ-2
Voltage	V	μ-1	Constant

Note: μ is scaling factor

Device scaling has several drawbacks in the form of Short Channel Effects (SCE), which are especially prevalent in Short Channel Devices (SCD). It is a kind of short-channel device if its channel length is equal to or less than its source and drain depletion junction layer width. As shown in Table II, there are a number of significant SCEs that influence performance. Since there is a large electric field present inside a tiny short channel gap when scaling is reduced, the SCE become more noticeable [9–15] as the device begins to work as expected. These impacts are mostly caused by two distinct phenomena.

1. Changes to the threshold voltage were made.
2. limitations imposed by the peculiarities of electron drift.

The notion of multi-gate, one of which is the double-gate MOSFET configuration, was born out of the need to reduce the limits imposed by single-gate Si-based MOSFETs while simultaneously investigating other channel materials and device structures (DG-MOSFET). DG-MOSFET is a device that uses two gates at the same time. In order to maximise gate control over the channel and increase gate coupling, these two gates are located on opposite sides of the device and separated by gate oxide of constant or variable thickness, as shown in Figure 3. This results in better current in the drain when fringing electric field lines move from the drain terminal to the source terminal. We must supply a voltage between the gate terminal and the source terminal (VGS) larger than or equal to the threshold voltage (VTH), i.e. VGS VTH, before electrons may travel in this

device. This is due to a rise in electron energy level [16-22] that occurs after delivering VGS VTH, resulting in an exponential increase in injection electron (electromagnetic flow in an N-type channel and a reversible flow in a P-type channel).

Research in this work focuses on the distinct double-gate MOSFETs in terms of channel material configuration, structural orientation, and potential applications. There are four additional parts in total on the remaining paper. Second, we'll take a look at traditional simulations of double-gate MOSFETs using various channel materials done by various researchers in the past, as well as actual uses of those simulations. The last portion of the paper will be presented in the third segment. In the fourth segment, we'll talk about the scope of the project. Finally, we get to the conclusion of the references section of this work.
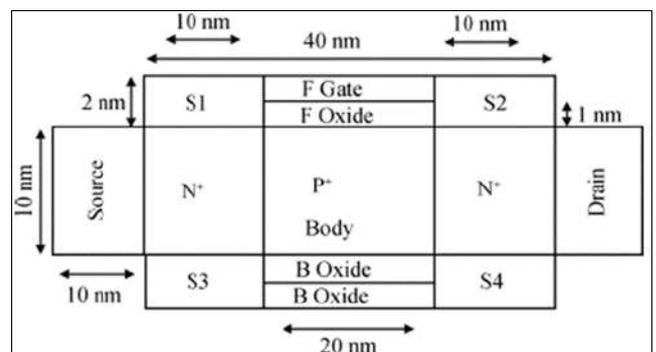

Fig 3: Double-Gate Configuration of MOSFET

Table 2: Short Channel Effects

Short Channel Effect	Reason
Gate Induced Drain Lowering (GIDL)	Off-state leakage current flows through the substrate-to-drain connection when gate biasing is done either at zero or negative voltage, since the depletion zone underneath the gate and drain overlaps.
Drain Induced Barrier Lowering (DIBL)	No matter whether the gate voltage is lower than the threshold voltage, electrons may flow freely between the source and drain even if the drain voltage is raised.
Surface Scattering	Collisions with other electrons, which travel faster into the depletion zone, cause additional surface scattering due to the roughness of this region's topography, which in turn accelerates these electrons.
Saturation Velocity	Saturation current flows due to carrier velocity instead of the pinch off point when MOSFETs are running in saturation mode and the bias voltage is not dropped, resulting in reduced trans conductance.
Hot Electron Effect	High electric fields in the depletion area cause electrons trapped in the oxide layer to accumulate charge, resulting in a rise in threshold voltage.
Threshold Voltage Roll Off	Because the channel lengths of short-channel devices are on a par with the widths of the depletion junction layers of the sources and drains, the electric field pattern created by the gate is 2D, lowering the threshold voltage for MOSFET functioning.
Punch Through	Depletion regions combine in short channel devices, causing an unregulated flow of current that cannot even be controlled by gate bias.
Oxide Tunneling Effect	For short channel devices, a strong electric field in the depletion zone causes a drop in the thickness of the oxide layer, which in turn increases the flow of current in the gate.
Carrier Mobility Degradation	When a strong electric field is present in the depletion zone, electrons are propelled to the depletion region, where they collide, and this reduces the surface mobility.
Parasitic Resistance	As the channel length reduces, parasitic resistance directly affects on-current and must be maintained low in short channel devices.
Parasitic Capacitance	A low on-current is hampered by parasitic capacitance, which is present in short-channel devices. This parasitic capacitance worsens with decreasing channel length.
Sub Threshold Leakage Current	When the gate voltage is smaller than the threshold voltage, a weak inversion conduction area is formed by the Hot Electron Effect, resulting in a flow of diffusion current between the drain and source.
Reverse Bias Leakage Current	The flow of reverse bias current between Because of the junction area, MOSFETs in the reverse bias or off state have shown to have drain-source and substrate problems.

Literature review

Double-gate MOSFET simulations based on various channel materials used by various researchers are discussed in this part, along with the practical uses of these simulated designs. For the purposes of this article, the various materials and gate configurations that have been employed so far have been summarised. Table- III

Table 3: Different channel materials, Gate configuration and Applications

References	Channel Materials and Gate Configuration	Application
[22]	Si0.2Ge0.8	Thermoelectric Applications
[23]	Si1-xGex	Source Step-FinFET and Inverter Applications
[24-25]	SiGe	In order to improve the ballistic carrier's velocity, optical interconnect applications that need high speed and high volume
[26]	Si0.75Ge0.25	On-State Current Applications with Improved Channel Controllability
[27]	Graphene Nanoribbon	Applications in DNA and Gas Sensing
[28]	Si Nanowire	Amplifiers for Low Noise
[29]	Ge Nanowire	High Mobility Channel Applications
[30]	Nanoscale Ge	High Speed and High Mobility Junction less Configuration Applications
[31]	Nanoscale Si	Low Power and Tunnel FET Applications
[32]	Analytical Model	Subthreshold Region Applications
[33]	Fully Depleted SOI	Radio Frequency Applications
[34]	Vertical Slit	3-DM Integration Applications
[35]	Gate All Around	6-Transistor SRAM Cell Applications
[36]	β-Ga2O3, HfO2 Gate Dielectric	High Power and High Temperature Electronic Devices
[37]	Heterogeneous Dielectric-Gate All Around-Tunnel	Improving Device Reliability Applications
[38]	Gaussian Like Doping	Optimization Peak Doping Concentration Applications
[39]	Doping Dependent Stack Channel	Multiple Threshold Voltage FinFET Configuration Applications
[40]	Negative Capacitance	Energy Delay Tradeoffs in Low Power Region Switching Applications
[41]	Heterojunction Tunnel Compact Model	Optimize Tunnel Logic Inverter Applications
[42]	2D Short Channel Semiconductor Material IV Model	Sub Threshold and Velocity Saturation Improvement Applications
[43]	III-V Compound Semiconductors	High Speed and Electrostatic Scaling Behavior Applications
[43]	InGaSb	P-Channel MOSFETs Applications
[43-44]	InGaAs	Current Amplification, N-Channel Configuration and Wide Channel Interactions Applications
[44]	Novel Dual Gate (In0.75Ga0.25As)	Current Amplification and Wide Channel Interactions Applications
[45]	Optimum High K-Oxide Ultra Scaling	Improving Gate Leakage Ultra-Scaled Applications
[46]	Dual Material	High Performance Circuit Applications
[46]	Dual Material Graded Channel	Threshold Voltage Applications
[47]	SiGe/SiC Asymmetric Dual-K Spacer	High Performance and Robust 6-Transistor (FinFET) SRAM Cell

		Applications
[48]	Sub 100 nm Tunnel FET	DRAM Applications
[49]	GaN	Commercial Power Devices and Converter Design Applications
[50]	Arsenic (As) and Antimony (Sb)	High Performance Digital Applications
[51]	SiGe Shell	Ultrathin P-FinFET Applications
[52]	Ge Ferroelectric	Current Drivability Applications
[53]	Schottky Barrier	Leakage Current Improvement Applications
[54]	Cylindrical Surrounding Gate	Improved Hot Carrier Reliability and Radio Frequency Applications
[55]	Gate Engineering	Stack Arrangement and Lateral Placed Gate Applications
[55]	Channel Engineering	Pocket Engineering and Graded Doping Applications
[55]	Work Engineering	Diminishing Threshold Voltage Applications

Upon examination of the above table, it is clear that the research work carried out by researchers in channel materials such as Si0.2Ge0.8, Si1-xGex, SiGe, and Si0.75Ge0.25 can be a watershed moment in the future, as Ge in the future can be a better alternative for Si based integrated circuits, as Ge not only possesses both balanced and high electron mobility and hole mobility, but it also has a higher density of states in comparison to the other III–V Upon examination of the above table, it is clear that the research work carried out by researchers in channel materials such as Si0.2Ge0.8, Si1-xGex, SiGe, and Si0.75Ge0.25 can be a watershed moment in the future, as Ge in the future can be a better alternative for Si based integrated circuits, as Ge not only possesses both balanced and high electron mobility and hole mobility, but it also has a higher density of states in comparison to the other III–V.

Result analysis
Table IV summarises the performance characteristics for the various channel materials and Table V summarises the comparative findings for the double gate MOSFET and single gate MOSFET studied in this work. Double-gate MOSFETs outperform single-gate MOSFETs in terms of performance, and their many benefits suggest that they should be pursued for future applications. DG MOSFETs have a phenomenally tiny structure, which has a promising future in the area of VLSI design from the previous explanation. Reliability is extremely high, costs are reasonable, power consumption is low, and it uses a tiny amount of space, which leads to better gate electrostatic control of the conducting channel and dynamic voltage management, thereby providing greater performance. Nanoscale CMOS circuits, which are in high demand in the electronics and communication industries, would benefit greatly from this technology, which meets all of the standards for IC design. So it can be inferred that the future of these gated communities will be bright in the years ahead.

Table 4: Different Channel materials used for making comparison between Single Gate MOSFET and Double Gate MOSFET

Channel Materials	Used in Single Gate Configuration of MOSFET	Used in Double Gate Configuration of MOSFET
Si	Yes	Yes
SiGe	Yes	Yes
InGaSb	Yes	Yes
InGaAs	Yes	Yes
Si0.75Ge0.25	Yes	Yes
Si0.2Ge0.8	Yes	Yes

Table 5: Comparison between Single Gate Configuration of MOSFET and Double Gate Configuration of MOSFET for different channel materials

Performance Parameters	Single Gate Configuration of MOSFET	Double Gate Configuration of MOSFET
Electron Mobility of Channel	In Order of 1500 cm^2/Vs	In Order of 3420 cm^2/Vs
Hole Mobility of Channel	In Order of 450 cm^2/Vs	In Order of 1610 cm^2/Vs
Bandgap of Channel Material	Multiple of 1.12 eV	Multiple of 0.66 eV
Electric Field	Requires Break Below field of ~ 10^7 V/cm	Requires Break Below field of ~ 10^5 V/cm
Saturation Velocity	Multiple of 107 cm/s	Multiple of $6*106$ cm/s
Off State Leakage Current	Greater than 1nA/um	Less than 1nA/um
Drive Current Delay	Higher Order Range of 0.1 ns	Lower Order Range of 0.05 ns
Power Dissipated	Between 0.5 J/s to 0.7 J/s	Between 0.1 J/s to 0.3 J/s
Threshold Voltage	Between 0.35 V to 0.45 V	Between 0.1 V to 0.3 V

Conclusion
This conclusion can be drawn after analysing all the theoretical work done by different researchers theoretically in terms of different performance parameters for different channel materials and comparing the double gate MOSFET configuration with single gate MOSFET configuration in terms of different performance parameters for different channel materials. Double-gate MOSFETs are expected to outperform single-gate MOSFETs in various performance parameters for various channel materials in the future, according to previous theoretical and experimental work, and this device configuration has a promising future as a potential replacement for single-gate MOSFETs in the near future.

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